General Purpose Timers

ICM7555, ICM7556

The ICM7555 and ICM7556 are CMOS RC timers providing significantly improved performance over the standard SE/NE 555/556 and 355 timers, while at the same time being direct replacements for those devices in most applications. Improved parameters include low supply current, wide operating supply voltage range, low Threshold, $\overline{\text{Trigger}}$ and $\overline{\text{Reset}}$ currents, no crowbarring of the supply current during output transitions, higher frequency performance and no requirement to decouple Control Voltage for stable operation.

Specifically, the ICM7555 and ICM7556 are stable controllers capable of producing accurate time delays or frequencies. The ICM7556 is a dual ICM7555, with the two timers operating independently of each other, sharing only V+ and GND. In the one shot mode, the pulse width of each circuit is precisely controlled by one external resistor and capacitor. For astable operation as an oscillator, the free running frequency and the duty cycle are both accurately controlled by two external resistors and one capacitor. Unlike the regular bipolar SE/NE 555/556 devices, the Control Voltage terminal need not be decoupled with a capacitor. The circuits are triggered and reset on falling (negative) waveforms, and the output inverter can source or sink currents large enough to drive TTL loads, or provide minimal offsets to drive CMOS loads.

Features

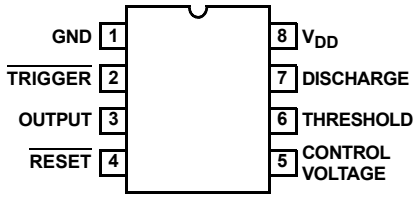
- Exact equivalent in most cases for SE/NE 555/556 or TLC555/556
- Low supply current
  - ICM7555 . . . . . 60µA
  - ICM7556 . . . . . 120µA
- Extremely low input currents 20pA
- High speed operation 1MHz
- Guaranteed supply voltage range . . . . . 2V to 18V
- Temperature stability . . . . . 0.005%/°C at +25°C
- Normal reset function - no crowbarring of supply during output transition
- Can be used with higher impedance timing elements than regular 555/556 for longer RC time constants
- Timing from microseconds through hours
- Operates in both astable and monostable modes
- Adjustable duty cycle
- High output source/sink driver can drive TTL/CMOS
- Outputs have very low offsets, HIGH and LOW
- Pb-free (RoHS Compliant)

Applications

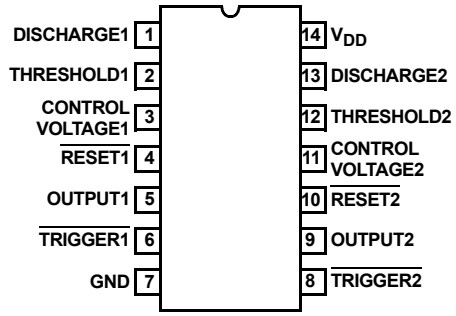
- Precision timing
- Pulse generation
- Sequential timing
- Time delay generation
- Pulse width modulation
- Pulse position modulation
- Missing pulse detector

Pin Configurations

ICM7555
(8 LD PDIP, SOIC)
TOP VIEW



ICM7556
(14 LD PDIP, CERDIP)
TOP VIEW



Ordering Information

PART NUMBER	PART MARKING	TEMP. RANGE (°C)	TAPE AND REEL (UNITS)	PACKAGE (RoHS COMPLIANT)	PKG. DWG. #
ICM7555CBAZ (Notes 2, 3)	7555 CBAZ	0 to +70		8 Ld SOIC	M8.15
ICM7555CBAZ-T (Notes 1, 2, 3)	7555 CBAZ	0 to +70	2.5k	8 Ld SOIC (Tape and Reel)	M8.15
ICM7555IBAZ (Notes 2, 3)	7555 IBAZ	-25 to +85		8 Ld SOIC	M8.15
ICM7555IBAZ-T (Notes 1, 2, 3)	7555 IBAZ	-25 to +85	2.5k	8 Ld SOIC (Tape and Reel)	M8.15
ICM7555IPAZ (Notes 2, 3)	7555 IPAZ	-25 to +85		8 Ld PDIP	E8.3
ICM7556IPDZ (Notes 2, 3)	ICM7556IPDZ	-25 to +85		14 Ld PDIP	E14.3
ICM7556MJD (**No longer available or supported**)	ICM7556MJD	-55 to +125		14 Ld Cerdip	F14.3

NOTES:

1. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see product information page for ICM7555, ICM7556. For more information on MSL, please see tech brief TB363.

Absolute Maximum Ratings

Supply Voltage . . . . . +18V
Input Voltage
  $\overline{\text{Trigger}}$, Control Voltage, Threshold,
  $\overline{\text{Reset}}$ (Note 4) . . . . . V+ +0.3V to GND -0.3V
Output Current 100mA

Operating Conditions

Temperature Range
  ICM7555C . . . . . 0°C to +70°C
  ICM7555I, ICM7556I . . . . . -25°C to +85°C
  ICM7556M . . . . . -55°C to +125°C

Thermal Information

Thermal Resistance (Typical, Notes 5, 6)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
14 Ld CERDIP Package	80	24
14 Ld PDIP Package*	115	46
8 Ld PDIP Package*	130	69
8 Ld SOIC Package	170	67

Maximum Junction Temperature (Hermetic Package) . . . . . +175°C
Maximum Junction Temperature (Plastic Package) . . . . . +150°C
Maximum Storage Temperature Range . . . . . -65°C to +150°C
* Pb-free PDIPs can be used for through-hole wave solder processing only. They are not intended for use in Reflow solder processing applications.

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

4. Due to the SCR structure inherent in the CMOS process used to fabricate these devices, connecting any terminal to a voltage greater than V+ +0.3V or less than V- -0.3V may cause destructive latch-up. For this reason it is recommended that no inputs from external sources not operating from the same power supply be applied to the device before its power supply is established. In multiple supply systems, the supply of the ICM7555 and ICM7556 must be turned on first.
5. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.
6. For θ_{JC}, the "case temp" location is taken at the package top center.

Electrical Specifications

Applies to ICM7555 and ICM7556, unless otherwise specified.

PARAMETER	SYMBOL	TEST CONDITIONS		T_A = +25°C			(Note 8) -55°C TO +125°C			UNIT
				MIN	TYP	MAX	MIN	TYP	MAX	
Static Supply Current	I_{DD}	ICM7555	V_{DD} = 5V		40	200			300	µA
			V_{DD} = 15V		60	300			300	µA
		ICM7556	V_{DD} = 5V		80	400			600	µA
			V_{DD} = 15V		120	600			600	µA
Monostable Timing Accuracy		R_A = 10k, C = 0.1µF, V_{DD} = 5V			2					%
							858		1161	µs
Drift with Temperature (Note 7)		V_{DD} = 5V						150		ppm/°C
		V_{DD} = 10V						200		ppm/°C
		V_{DD} = 15V						250		ppm/°C
Drift with Supply (Note 7)		V_{DD} = 5V to 15V			0.5			0.5		%/V
Astable Timing Accuracy		R_A = R_B = 10k, C = 0.1µF, V_{DD} = 5V			2					%
							1717		2323	µs
Drift with Temperature (Note 7)		V_{DD} = 5V						150		ppm/°C
		V_{DD} = 10V						200		ppm/°C
		V_{DD} = 15V						250		ppm/°C
Drift with Supply (Note 7)		V_{DD} = 5V to 15V			0.5			0.5		%/V
Threshold Voltage	V_{TH}	V_{DD} = 15V		62	67	71	61		72	% V_{DD}
Trigger Voltage	V_{TRIG}	V_{DD} = 15V		28	32	36	27		37	% V_{DD}
Trigger Current	I_{TRIG}	V_{DD} = 15V				10			50	nA
Threshold Current	I_{TH}	V_{DD} = 15V				10			50	nA
Control Voltage	V_{CV}	V_{DD} = 15V		62	67	71	61		72	% V_{DD}

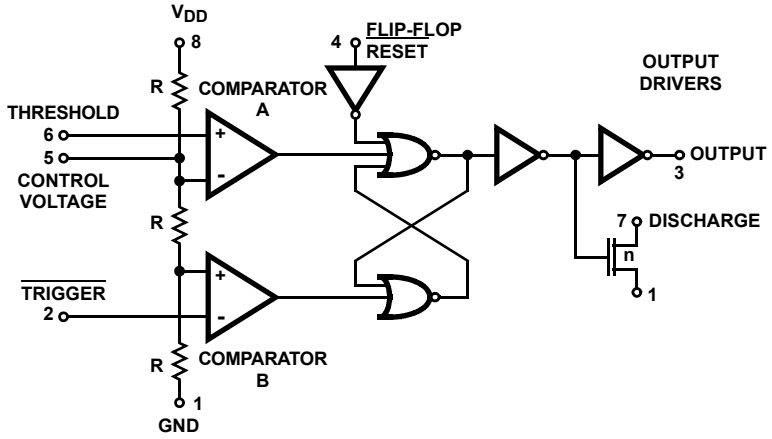
Electrical Specifications Applies to ICM7555 and ICM7556, unless otherwise specified. (Continued)

PARAMETER	SYMBOL	TEST CONDITIONS	T_A = +25°C			(Note 8) -55°C TO +125°C			UNIT
			MIN	TYP	MAX	MIN	TYP	MAX	
Reset Voltage	V_{RST}	V_{DD} = 2V to 15V	0.4		1.0	0.2		1.2	V
Reset Current	I_{RST}	V_{DD} = 15V			10			50	nA
Discharge Leakage	I_{DIS}	V_{DD} = 15V			10			50	nA
Output Voltage	V_{OL}	V_{DD} = 15V, I_{SINK} = 20mA		0.4	1.0			1.25	V
		V_{DD} = 5V, I_{SINK} = 3.2mA		0.2	0.4			0.5	V
	V_{OH}	V_{DD} = 15V, I_{SOURCE} = 0.8mA	14.3	14.6		14.2			V
		V_{DD} = 5V, I_{SOURCE} = 0.8mA	4.0	4.3		3.8			V
Discharge Output Voltage	V_{DIS}	V_{DD} = 5V, I_{SINK} = 15mA		0.2	0.4			0.6	V
		V_{DD} = 15V, I_{SINK} = 15mA						0.4	V
Supply Voltage (Note 7)	V_{DD}	Functional Operation	2.0		18.0	3.0		16.0	V
Output Rise Time (Note 7)	t_R	R_L = 10M, C_L = 10pF, V_{DD} = 5V		75					ns
Output Fall Time (Note 7)	t_F	R_L = 10M, C_L = 10pF, V_{DD} = 5V		75					ns
Oscillator Frequency (Note 7)	f_{MAX}	V_{DD} = 5V, R_A = 470Ω, R_B = 270Ω, C = 200pF		1					MHz

NOTES:

7. These parameters are based upon characterization data and are not tested.
8. Applies only to military temperature range product (M suffix).

Functional Diagram



NOTE: This functional diagram reduces the circuitry down to its simplest equivalent components. Tie down unused inputs.

FIGURE 1. FUNCTIONAL DIAGRAM

TRUTH TABLE

THRESHOLD VOLTAGE	$\overline{\text{TRIGGER}}$ VOLTAGE	$\overline{\text{RESET}}$	OUTPUT	DISCHARGE SWITCH
Don't Care	Don't Care	Low	Low	On
$>{}^2/_3(V+)$	$>{}^1/_3(V+)$	High	Low	On
$<{}^2/_3(V+)$	$>{}^1/_3(V+)$	High	Stable	Stable
Don't Care	$<{}^1/_3(V+)$	High	High	Off

NOTE: $\overline{\text{RESET}}$ will dominate all other inputs: $\overline{\text{TRIGGER}}$ will dominate over THRESHOLD.

Schematic Diagram

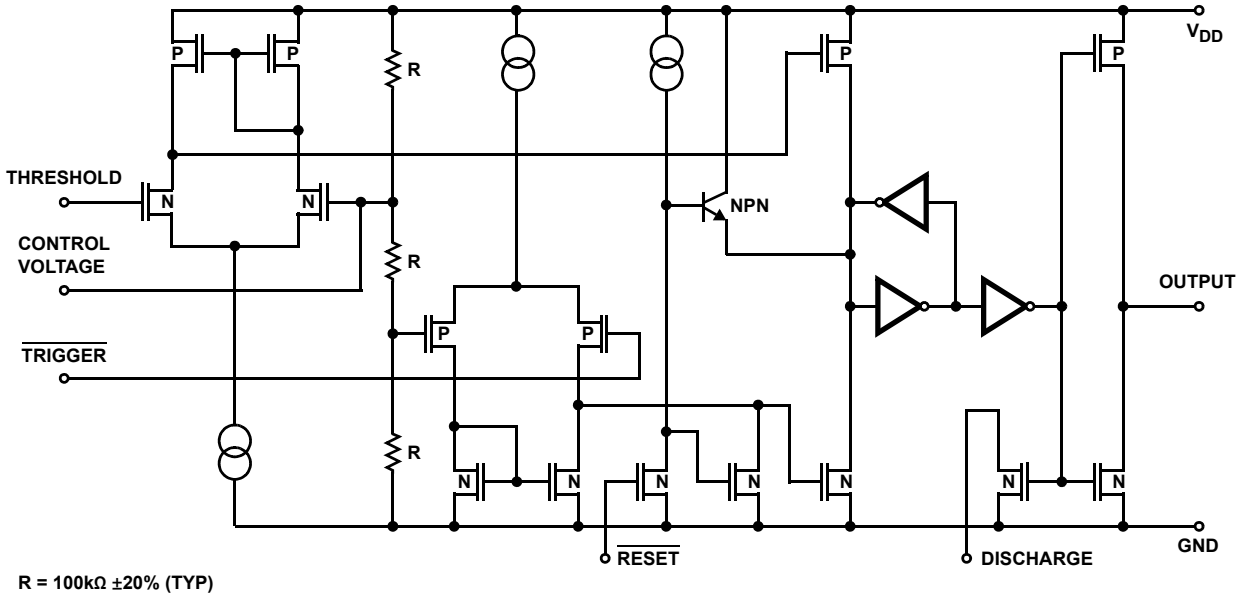


FIGURE 2. SCHEMATIC DIAGRAM

Application Information

General

The ICM7555 and ICM7556 devices are, in most instances, direct replacements for the SE/NE 555/556 devices. However, it is possible to effect economies in the external component count using the ICM7555 and ICM7556. Because the bipolar SE/NE 555/556 devices produce large crowbar currents in the output driver, it is necessary to decouple the power supply lines with a good capacitor close to the device. The ICM7555 and ICM7556 devices produce no such transients (see Figure 3).

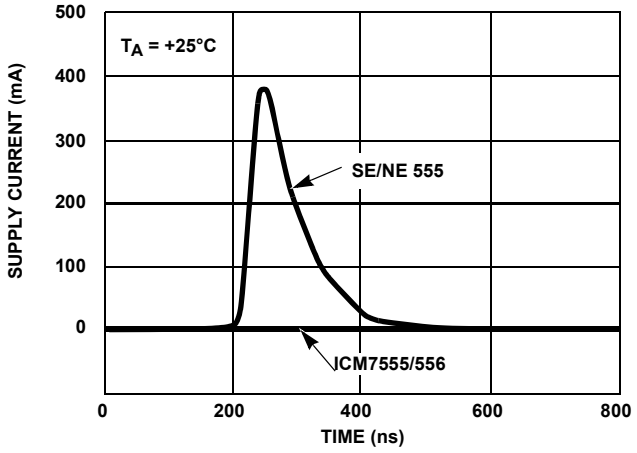


FIGURE 3. SUPPLY CURRENT TRANSIENT COMPARED WITH A STANDARD BIPOLAR 555 DURING AN OUTPUT TRANSITION

The ICM7555 and ICM7556 produce supply current spikes of only 2mA to 3mA instead of 300mA to 400mA and supply decoupling is normally not necessary. Also, in most instances, the Control Voltage decoupling capacitors are not required since the input impedance of the CMOS comparators on chip are very high. Thus, for many applications, two capacitors can be saved using an ICM7555 and three capacitors with an ICM7556.

POWER SUPPLY CONSIDERATIONS

Although the supply current consumed by the ICM7555 and ICM7556 devices is very low, the total system supply current can be high unless the timing components are high impedance. Therefore, use high values for R and low values for C in Figures 4, 5, and 6.

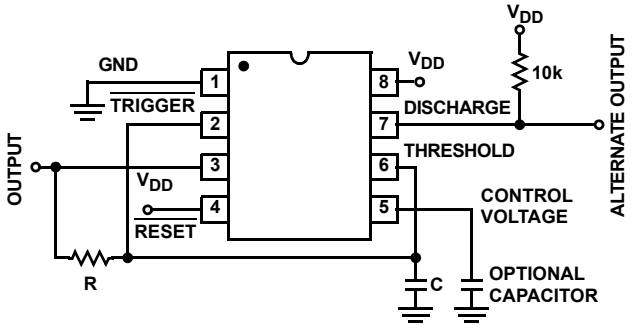


FIGURE 4. ASTABLE OPERATION

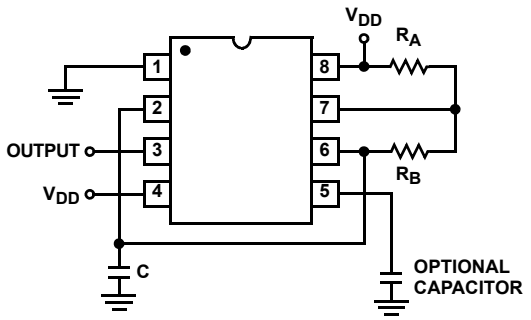


FIGURE 5. ALTERNATE ASTABLE CONFIGURATION

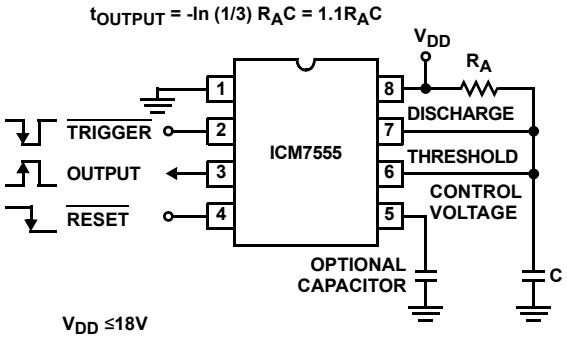


FIGURE 6. MONOSTABLE OPERATION

OUTPUT DRIVE CAPABILITY

The output driver consists of a CMOS inverter capable of driving most logic families including CMOS and TTL. As such, if driving CMOS, the output swing at all supply voltages will equal the supply voltage. At a supply voltage of 4.5V or more, the ICM7555 and ICM7556 will drive at least two standard TTL loads.

ASTABLE OPERATION

The circuit can be connected to trigger itself and free run as a multivibrator, see Figure 4. The output swings from rail-to-rail, and is a true 50% duty cycle square wave. Trip points and output swings are symmetrical. Less than a 1% frequency variation is observed over a voltage range of +5V to +15V.

$$f = \frac{1}{1.4\ RC} \quad \text{(EQ. 1)}$$

The timer can also be connected as shown in Figure 5. In this circuit, the frequency is as shown by Equation 2:

$$f = 1.44/(R_A + 2R_B)C \quad \text{(EQ. 2)}$$

The duty cycle is controlled by the values of R_A and R_B, by Equation 3:

$$D = (R_A + R_B)/(R_A + 2R_B) \quad \text{(EQ. 3)}$$

MONOSTABLE OPERATION

In this mode of operation, the timer functions as a one-shot (see Figure 6). Initially the external capacitor (C) is held discharged by a transistor inside the timer. Upon application of a negative $\overline{\text{Trigger}}$ pulse to pin 2, the internal flip-flop is set, which releases the short-circuit across the external capacitor and drives the Output high. The voltage across the capacitor now increases exponentially with a time constant t = R_AC. When the voltage across the capacitor equals $^2/_3$ V+, the comparator resets the flip-flop, which in turn discharges the capacitor rapidly and also drives the OUTPUT to its low state. $\overline{\text{Trigger}}$ must return to a high state before the OUTPUT can return to a low state.

CONTROL VOLTAGE

The Control Voltage terminal permits the two trip voltages for the Threshold and $\overline{\text{Trigger}}$ internal comparators to be controlled. This provides the possibility of oscillation frequency modulation in the astable mode or even inhibition of oscillation, depending on the applied voltage. In the monostable mode, delay times can be changed by varying the applied voltage to the Control Voltage pin.

$\overline{\text{RESET}}$

The $\overline{\text{Reset}}$ terminal is designed to have essentially the same trip voltage as the standard bipolar 555/556, i.e., 0.6V to 0.7V. At all supply voltages it represents an extremely high input impedance. The mode of operation of the $\overline{\text{Reset}}$ function is, however, much improved over the standard bipolar SE/NE 555/556 in that it controls only the internal flip-flop, which in turn controls simultaneously the state of the Output and Discharge pins. This avoids the multiple threshold problems sometimes encountered with slow falling edges in the bipolar devices.

Typical Performance Curves

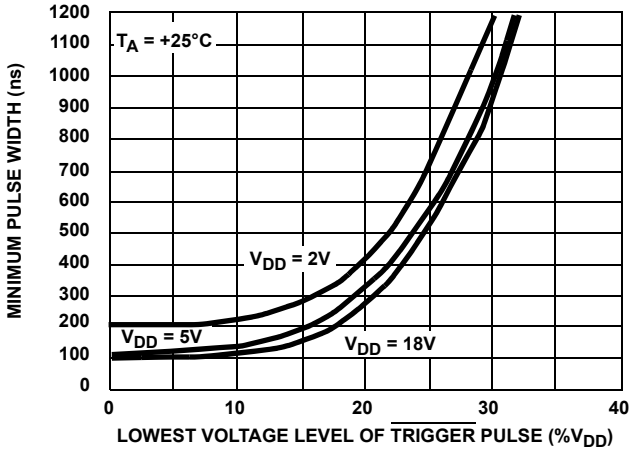


FIGURE 7. MINIMUM PULSE WIDTH REQUIRED FOR TRIGGERING

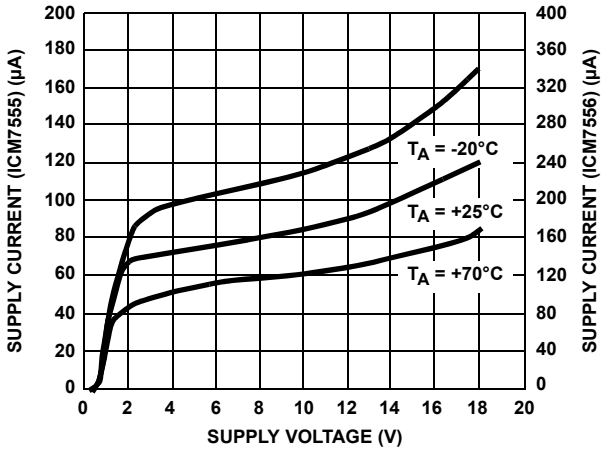


FIGURE 8. SUPPLY CURRENT vs SUPPLY VOLTAGE

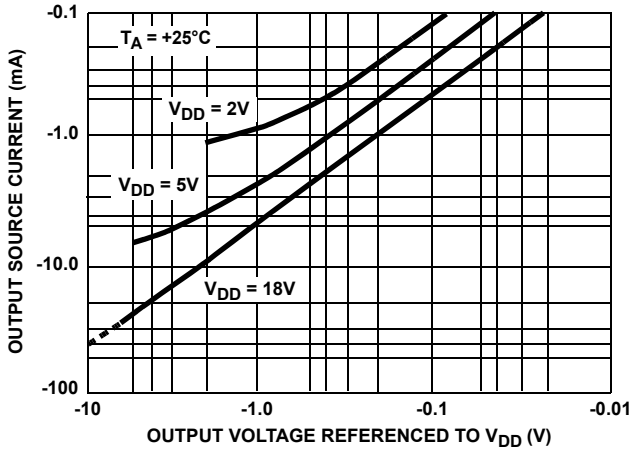


FIGURE 9. OUTPUT SOURCE CURRENT vs OUTPUT VOLTAGE

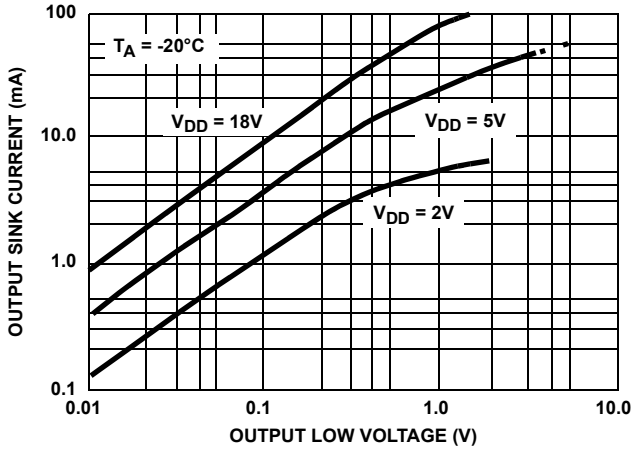


FIGURE 10. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

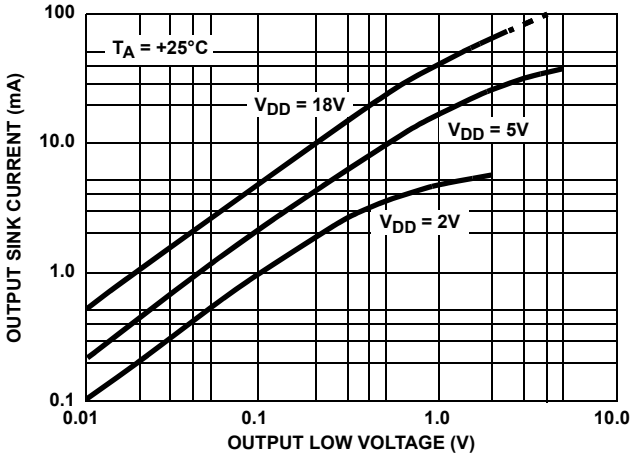


FIGURE 11. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

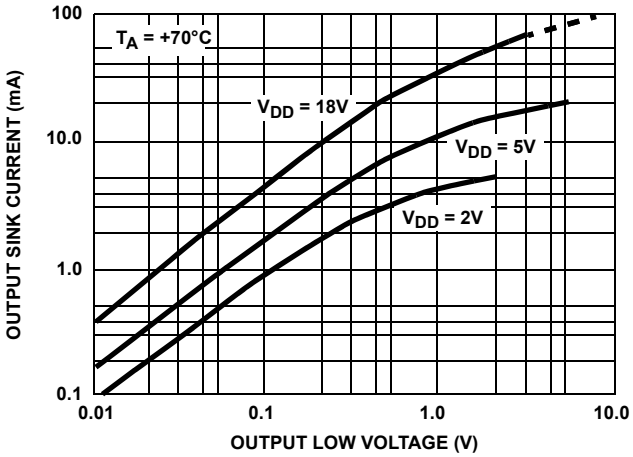


FIGURE 12. OUTPUT SINK CURRENT vs OUTPUT VOLTAGE

Typical Performance Curves (Continued)

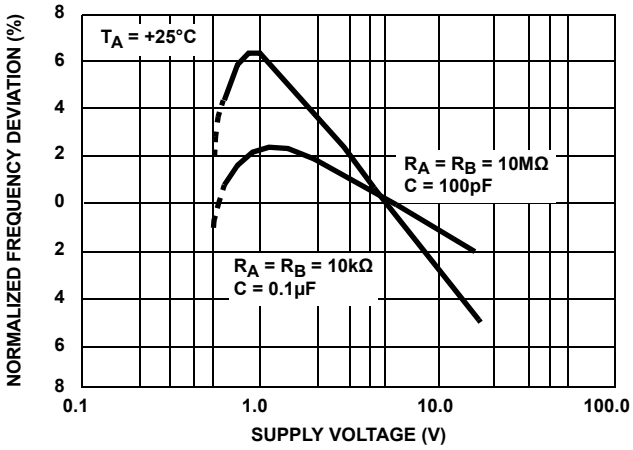


FIGURE 13. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs SUPPLY VOLTAGE

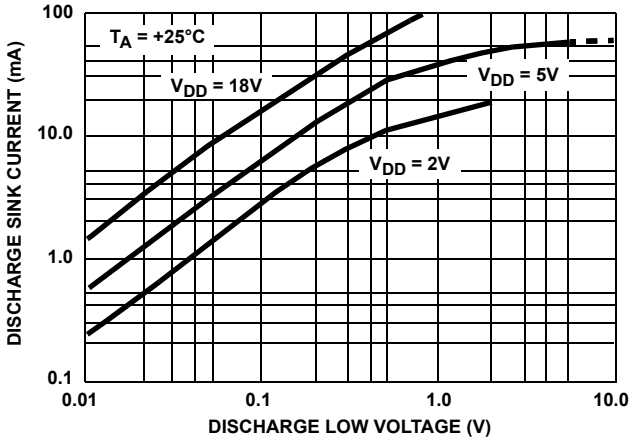


FIGURE 14. DISCHARGE OUTPUT CURRENT vs DISCHARGE OUTPUT VOLTAGE

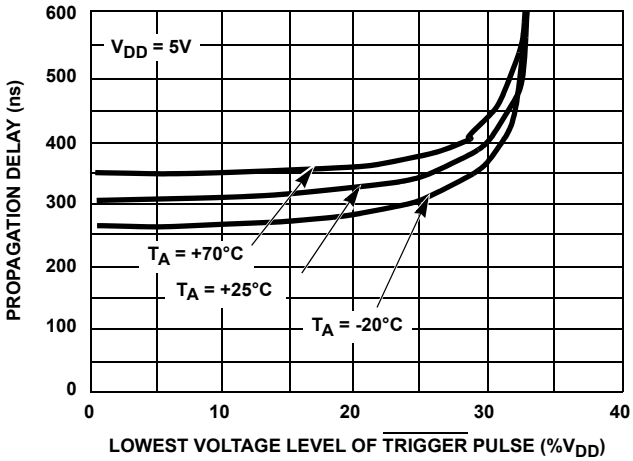


FIGURE 15. PROPAGATION DELAY vs VOLTAGE LEVEL OF TRIGGER PULSE

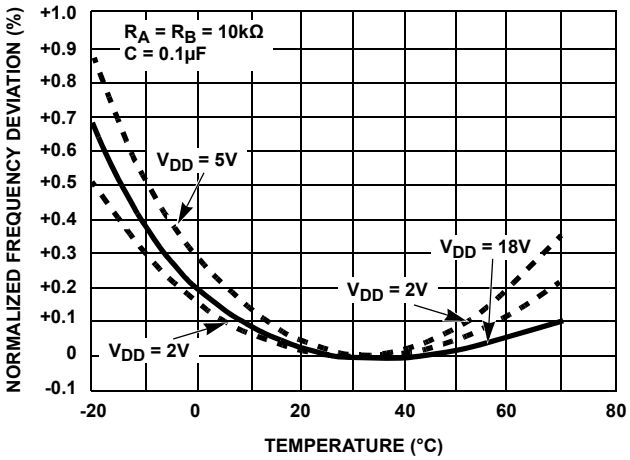


FIGURE 16. NORMALIZED FREQUENCY STABILITY IN THE ASTABLE MODE vs TEMPERATURE

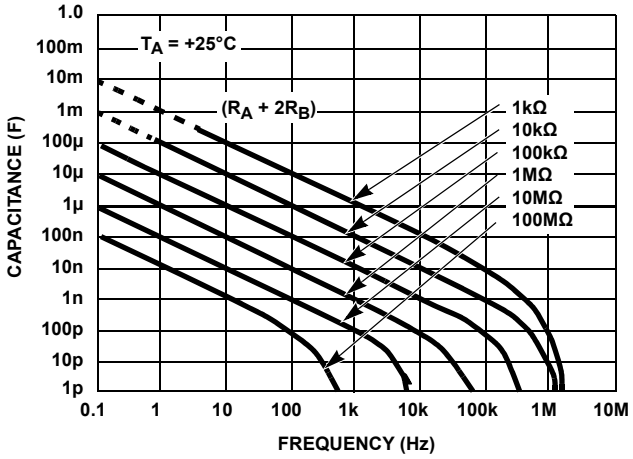


FIGURE 17. FREE RUNNING FREQUENCY vs R_A, R_B AND C

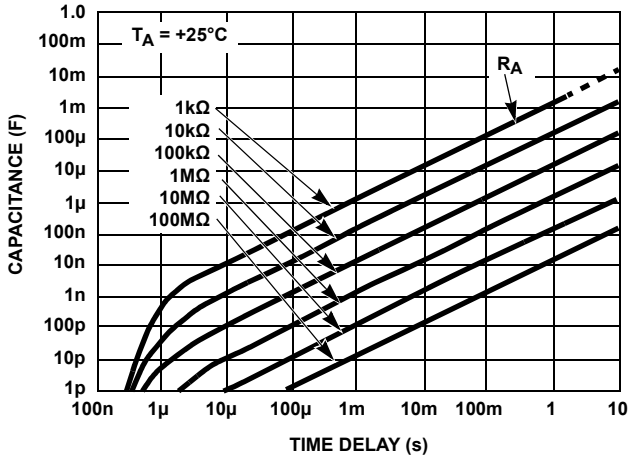


FIGURE 18. TIME DELAY IN THE MONOSTABLE MODE vs R_A AND C

Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to the web to make sure that you have the latest revision.

DATE	REVISION	CHANGE
June 28, 2016	FN2867.10	Converted to new datasheet template. Updated 14 Ld PDIP “Pin Configuration” on page 1 by adding “1” or “2” to pins that have same name. Updated “Thermal Information” on page 3 by removing Maximum Lead Temperature and Adding T_{JC} values with corresponding note. Updated “Ordering Information” table on page 2 by removing obsoleted parts, adding Tape and Reel option column, adding MSL note and numbering notes accordingly. Updated POD M8.15 to most current version. POD changes are as follows: Changed in Typical Recommended Land Pattern the following: 2.41(0.095) to 2.20(0.087) 0.76 (0.030) to 0.60(0.023) 0.200 to 5.20(0.205) Updated to new POD format by removing table and moving dimensions onto drawing and adding land pattern

About Intersil

Intersil Corporation is a leading provider of innovative power management and precision analog solutions. The company's products address some of the largest markets within the industrial and infrastructure, mobile computing and high-end consumer markets.

For the most updated datasheet, application notes, related documentation and related parts, please see the respective product information page found at www.intersil.com.

You may report errors or suggestions for improving this datasheet by visiting www.intersil.com/ask.

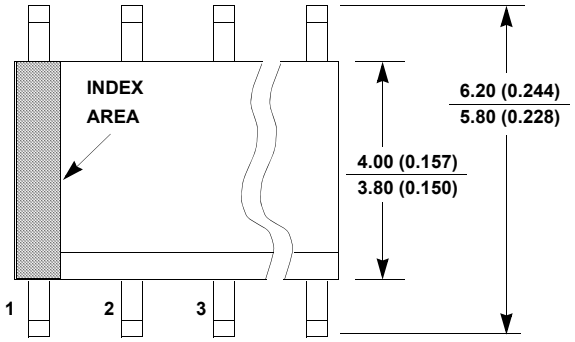
Reliability reports are also available from our website at www.intersil.com/support.

Package Outline Drawing

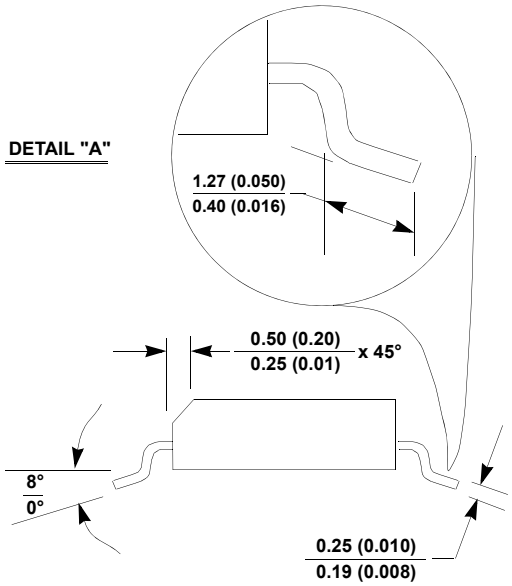
M8.15

8 LEAD NARROW BODY SMALL OUTLINE PLASTIC PACKAGE

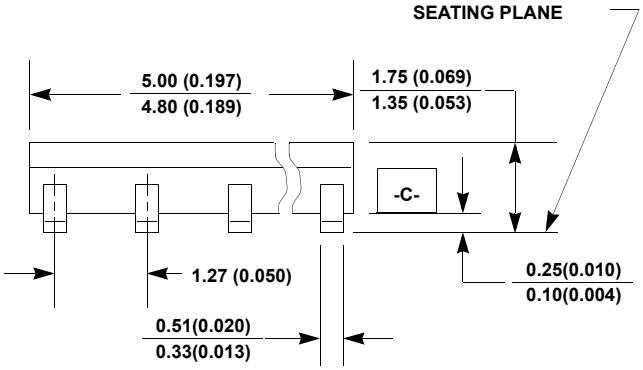
Rev 4, 1/12



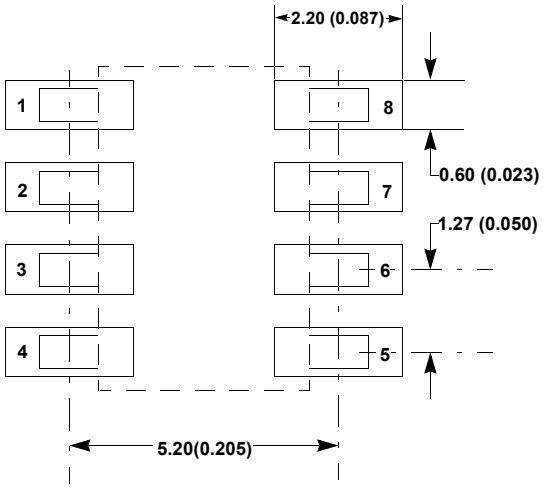
TOP VIEW



SIDE VIEW “B”



SIDE VIEW “A”

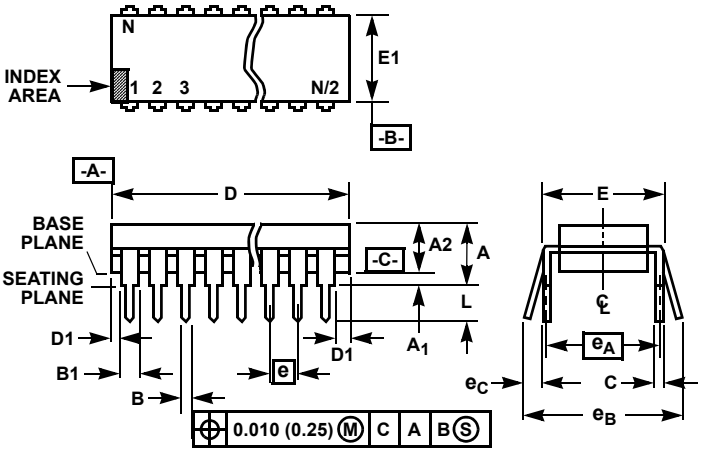


TYPICAL RECOMMENDED LAND PATTERN

NOTES:

1. Dimensioning and tolerancing per ANSI Y14.5M-1994.
2. Package length does not include mold flash, protrusions or gate burrs. Mold flash, protrusion and gate burrs shall not exceed 0.15mm (0.006 inch) per side.
3. Package width does not include interlead flash or protrusions. Interlead flash and protrusions shall not exceed 0.25mm (0.010 inch) per side.
4. The chamfer on the body is optional. If it is not present, a visual index feature must be located within the crosshatched area.
5. Terminal numbers are shown for reference only.
6. The lead width as measured 0.36mm (0.014 inch) or greater above the seating plane, shall not exceed a maximum value of 0.61mm (0.024 inch).
7. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
8. This outline conforms to JEDEC publication MS-012-AA ISSUE C.

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

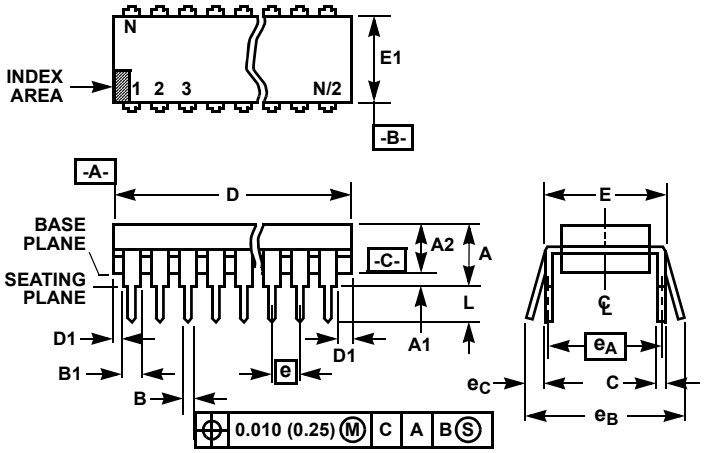
E8.3 (JEDEC MS-001-BA ISSUE D)

8 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8, 10
C	0.008	0.014	0.204	0.355	-
D	0.355	0.400	9.01	10.16	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	8		8		9

Rev. 0 12/93

Dual-In-Line Plastic Packages (PDIP)



NOTES:

1. Controlling Dimensions: INCH. In case of conflict between English and Metric dimensions, the inch dimensions control.
2. Dimensioning and tolerancing per ANSI Y14.5M-1982.
3. Symbols are defined in the "MO Series Symbol List" in Section 2.2 of Publication No. 95.
4. Dimensions A, A1 and L are measured with the package seated in JEDEC seating plane gauge GS-3.
5. D, D1, and E1 dimensions do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.010 inch (0.25mm).
6. E and e_A are measured with the leads constrained to be perpendicular to datum -C-.
7. e_B and e_C are measured at the lead tips with the leads unconstrained. e_C must be zero or greater.
8. B1 maximum dimensions do not include dambar protrusions. Dambar protrusions shall not exceed 0.010 inch (0.25mm).
9. N is the maximum number of terminal positions.
10. Corner leads (1, N, N/2 and N/2 + 1) for E8.3, E16.3, E18.3, E28.3, E42.6 will have a B1 dimension of 0.030 - 0.045 inch (0.76 - 1.14mm).

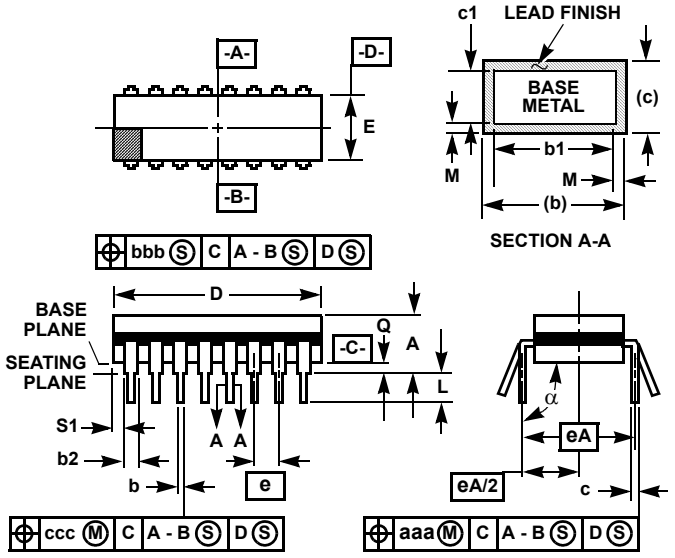
E14.3 (JEDEC MS-001-AA ISSUE D)

14 LEAD DUAL-IN-LINE PLASTIC PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.210	-	5.33	4
A1	0.015	-	0.39	-	4
A2	0.115	0.195	2.93	4.95	-
B	0.014	0.022	0.356	0.558	-
B1	0.045	0.070	1.15	1.77	8
C	0.008	0.014	0.204	0.355	-
D	0.735	0.775	18.66	19.68	5
D1	0.005	-	0.13	-	5
E	0.300	0.325	7.62	8.25	6
E1	0.240	0.280	6.10	7.11	5
e	0.100 BSC		2.54 BSC		-
e_A	0.300 BSC		7.62 BSC		6
e_B	-	0.430	-	10.92	7
L	0.115	0.150	2.93	3.81	4
N	14		14		9

Rev. 0 12/93

Ceramic Dual-In-Line Frit Seal Packages (CERDIP)



NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. This dimension allows for off-center lid, meniscus, and glass overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. Measure dimension S1 at all four corners.
8. N is the maximum number of terminal positions.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

F14.3 (MIL-STD-1835 GDIP1-T14 (D-1, CONFIGURATION A)

14 LEAD CERAMIC DUAL-IN-LINE FRIT SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	5
E	0.220	0.310	5.59	7.87	5
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	6
S1	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2, 3
N	14		14		8

Rev. 0 4/94